Remarks

The Official Action rejected claims 1-29. Claims 1-29 remain pending. Applicant respectfully requests allowance of the pending claims in light of the points that follow.

Claim Rejections – 35 USC § 102

The Official Action rejected claims 1-6, 13-18, and 25-27 under 35 USC 102(b) as being anticipated by Watkins et al (US 5,220,512). Applicant respectfully requests the rejection of the pending claims to be withdrawn.

As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claims 1 and 13

Each of claims 1 and 13 require using a logic design element in a logic design, performing a simulation of the logic design that includes simulating the logic design element and **having the logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data relate to the logic design element.** The Official Action appears to rely on FIGs 2, 3, and 4 and the description provided in col. 8, lines 4-6, col.1, lines 15-49, col. 5, lines 5-10, col. 10, lines 53-68, and col. 11, lines 1-4 to teach the limitations of claims 1 and 13. However, Watkins does not appear to teach using a logic design element in a logic design, performing a simulation of the logic design that includes simulating the logic design element and having the logic design element automatically collect instrumentation data

during the simulation, wherein the instrumentation data relate to the logic design element.

In contrast, Watkins teaches (in col. 5, lines 5-10) enabling a user to perform simulator setup on the schematic diagram by using point and select techniques to identify items to be simulated, input values, override values, and points to be monitored. The points to be monitored refer to specific points of interest in the logic schematic and signal levels of these points are generally monitored to verify the appropriateness of logic design. For example, the logic design verification process may provide input values for which the desired output at different points (points to be monitored) is known. The actual output generated at points to be monitored is compared with the desired outputs to detect whether the logic design would operate as desired.

Watkins discloses (in col. 10, lines 53-63) an editor display 300 of FIG. 3 displaying the output at different points to be monitored (e.g., 324, 326, and 332) for different input values of CP and CD. A state table 318 depicts the actual output at the monitored points or nodes/nets for various combinations of input values by performing simulation. The data depicted in table 318 is built (as described in col. 11, lines 1-4) by iterative invocations of the simulator by a schematic editor according to user specified monitoring and simulation conditions. As it may be observed, the data depicted in the state table 318 is representative of logic design verification and does not represent instrumentation data such as the utilization statistics of the logic design elements. Also, the state table 318 is populated by iterative invocations of the simulator and the data in the state table is not collected automatically.

Watkins does not disclose automatically collecting instrumentation data relating to the logic design element during the simulation. The instrumentation data may represent, for example, utilization statistics that may provide insight into system architecture. Watkins appears to provide an improved ECAD system in which the characteristics of schematic editor, schematic compiler, and simulator are all presented to the user in a fashion such that they appear as a single, integrated function. Since Watkins does not appear to teach each and every limitation of claims 1 and 13, Watkins does not anticipate the invention of claims 1 and 13. Applicants respectfully request the rejection of claims 1 and 13 be withdrawn.

Claims 2-6 and 14-18

Each of claims 2-6 and 14-18, respectively, depend from one of claims 1 and 13. Accordingly, each of claims 2-6 and 14-18 are allowable for at least the reasons given above. Applicant respectfully request allowance of claims 2-6 and 14-18.

Claim 25

Claim 25 requires a simulation module that is structured and arranged to perform a simulation of a logic design that includes a logic design element and a collection module that is integrated with the logic design element and that is structured and **arranged to automatically collect instrumentation data relating to the logic design element during the simulation**. The Official Action appears to rely on FIGs 2, 3, and 4 and the description provided in col. 8, lines 4-6, col.1, lines 15-49, col. 5, lines 5-10, col. 10, lines 53-68, col. 11, lines 1-4, and col. 7, lines 17-27 to teach the limitations of claim 25.

Watkins discloses (in Fig. 2, element 224 and description provided in col. 7, lines 17-27) a logic simulator after performing a simulation according to user's specification places the result of simulation in a data structure, signals the editor, and places the data on the display per user's specification. Such a simulation can be performed as a complete simulation run or in stepped simulation run and the results may be displayed once completely after the complete simulation run or append the results after each stepped simulation run. However, Watkins is silent on a logic design element arranged to automatically collect instrumentation data relating to the logic design element during the simulation as required by claim 25. Applicants respectfully request the rejection of claim 25 be withdrawn.

Claim 26-27

Each of claims 26-27 depend from claim 25. Accordingly, each of claims 26-27 are allowable for at least the reasons given above. Applicant respectfully request allowance of claims 26-27.

Claim Rejections – 35 USC § 103(a) (Watkins/Sharma)

The Official Action further rejected claims 7-9, 19-21, and 28 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) in view of Sharma (US 5,978,574). Applicants respectfully request allowance of claims 7-9, 19-21, and 28 in light of the points that follow.

Claims 7 and 19

Each of claims 7 and 19 require a logic design element to include a FIFO memory and **having the logic design element automatically collect the**

instrumentation data to include having the FIFO memory automatically collects the instrumentation data during the simulation, with the instrumentation data relating to the FIFO memory. The Official Action appears to rely on FIG. 3 and the description provided in col. 5, lines 5-10, col. 10, lines 53-68, and col. 11, lines 1-4 of Watkins and FIG. 2 and FIG. 3 and the description provided in col. 1, lines 63-67, col. 2, lines 10-14, and lines 31-36 of Sharma to teach the limitations of claims 7 and 19.

As described above, Watkins does not teach a logic design element that can automatically collect the instrumentation data during simulation. Sharma teaches (in col. 1, lines 63-67) that typical designs comprise FIFOs and the entities placing entries into the FIFO queue is regarded as a producer and the entities removing entries from the FIFO queue is regarded as a consumer. Sharma teaches (in col. 2, lines 10-14 and lines 31-36) that the traditional approach to verify queue flow-control is by simulation, emulation, or post silicon verification and further teaches that hardware emulations cover more cases than software simulation and even the hardware emulation does not guarantee that all cases are verified in the various queues. However, Sharma is silent on using a FIFO to automatically collect instrumentation data corresponding to the FIFO during simulation.

Watkins and Sharma, together or individually, do not teach all the limitations of claims 7 and 19. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Sharma with the art of Watkins to come up with the invention covered by the scope of claims 7 and 19 of the instant application. Applicants respectfully request the rejection of claims 7 and 19 be withdrawn.

Claims 8-9 and 20-21

Each of claims 8-9 and 20-21 respectively depend from one of claims 7 and 19. Accordingly, each of claims 8-9 and 20-21 is allowable for at least the reasons given above. Applicant respectfully request allowance of claims 8-9 and 20-21.

Claim 28

Claim 28 depends from claim 25 and is allowable for at least the reasons given above. Also, the description provided with reference to Fig. 3, col. 5, lines 5-10, col.10, lines 53-68, col. 11, lines 2-4 of Watkins and Fig. 2, col.1, lines 63-67 and col. 2, lines 10-14 and lines 31-36 of Sharma does not teach every limitation disclosed in claim 28. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Sharma with the art of Watkins to come up with the invention covered by the scope of claim 28 of the instant application. Applicants respectfully request the rejection of claim 28 be withdrawn.

Claim Rejections – 35 USC § 103 (Watkins/Mitchel)

The Official Action further rejected claims 10-12, 22-24, and 29 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) in view of Mitchell (US 5,646,553). Applicants respectfully request allowance of claims 10-12, 22-24, and 29 in light of the points that follow.

Claims 10 and 22

Each of claims 10 and 22 require a logic design element to include a tri-state bus and having the logic design element automatically collect the instrumentation data to

include having the tri-state bus automatically collects the instrumentation data during the simulation, with the instrumentation data relating to the tri-state bus. The Official Action appears to rely on the description provided in col. 7, lines 12-17 of Watkins and abstract, FIG. 1 and Col. 1 lines 45-50 of Mitchell to teach the limitations of claims 10 and 22.

Watkins teaches (in Col. 7 lines 12-17) receiving a command from a user, relaying the command, from an editor, to a simulator, performing simulation according to the commands, and storing the simulation results in a data structure. However, Watkins is silent on automatically collecting the instrumentation data, of a logic design element, during simulation. Mitchell teaches (in the abstract and col. 1 lines 45-50) to avoid contention by shutting off each device's output enable early, so that it is guaranteed to no longer drive the line by the time any other device beings to drive the line. To this end, Mitchell discloses activating the enable signal on the leading edge of the bus clock and deactivating the enable signal, at a delayed half phase clock edge, to avoid contention. However, Mitchell is silent on automatically collecting the instrumentation data of a tri-state bus during simulation.

Watkins and Mitchell, together or individually, do not teach all the limitations of claims 10 and 22. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Mitchell with the art of Watkins to come up with the invention covered by the scope of claims 10 and 22 of the instant application. Applicants respectfully request the rejection of claims 10 and 22 be withdrawn.

Claims 11-12 and 23-24

Each of claims 11-12 and 23-24 respectively depend from one of claims 10 and 22. Accordingly, each of claims 11-12 and 23-24 is allowable for at least the reasons given above.

Claim 29

Claim 29 depends from claim 25 and is allowable for at least the reasons given above. Also, the description provided with reference to col. 7, lines 12-17 of Watkins and Fig. 1 and abstract of Mitchell does not teach every limitation disclosed in claim 29 of the instant application. Thus, there would be no motivation and/or it would not have been obvious to a person having ordinary skill in the art to use the art of Mitchell with the art of Watkins to come up with the invention covered by the scope of claim 29 of the instant application. Applicants respectfully request the rejection of claim 29 be withdrawn.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicants submit that the application is in condition for allowance. Reconsideration is requested, and allowance of the pending claims is earnestly solicited. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities, which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

Date: 9/6/05

Gregory D. Caldwell
Reg. No. 39,926

c/o Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1030
408-720-8300